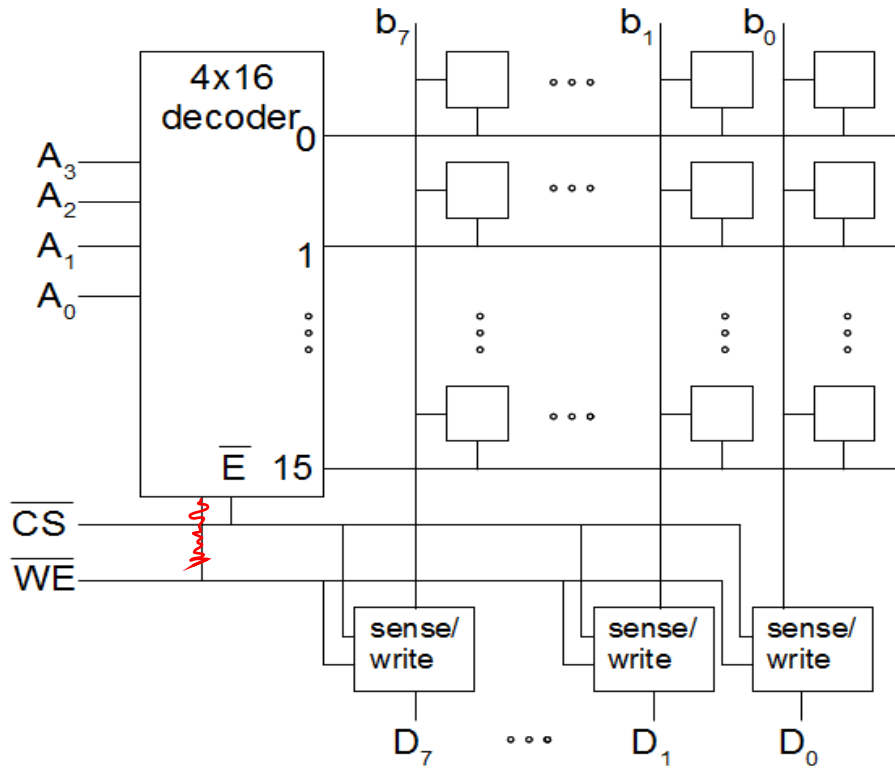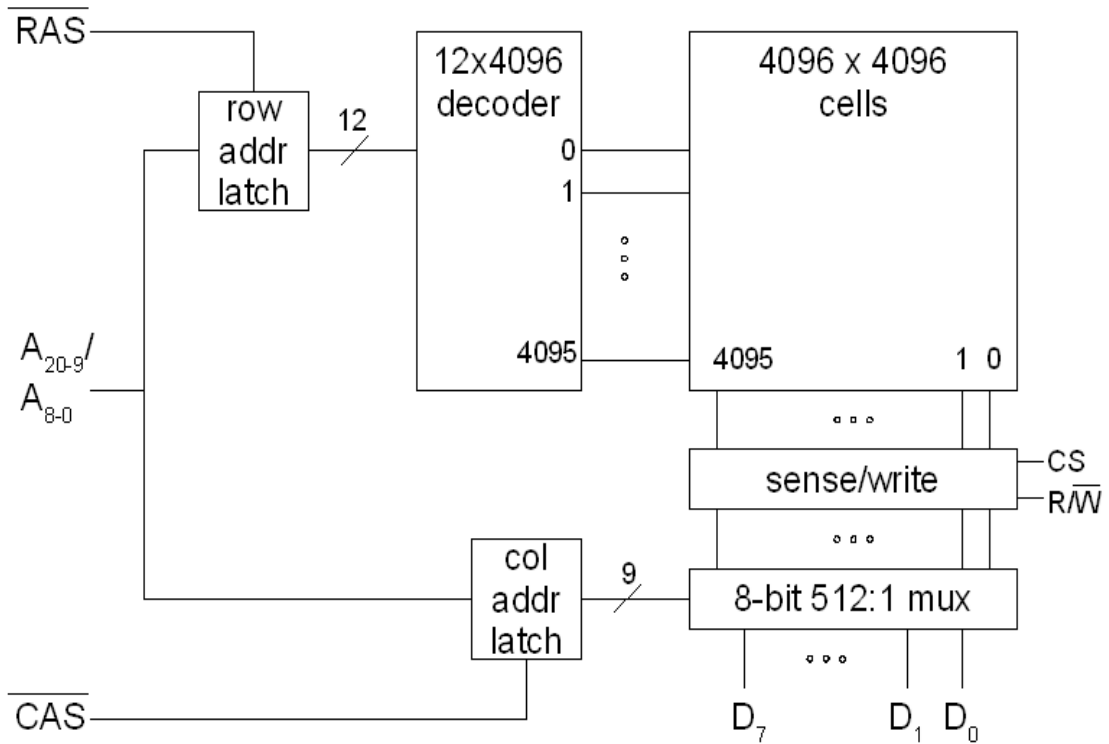16 x 8 bit memory (internal view)
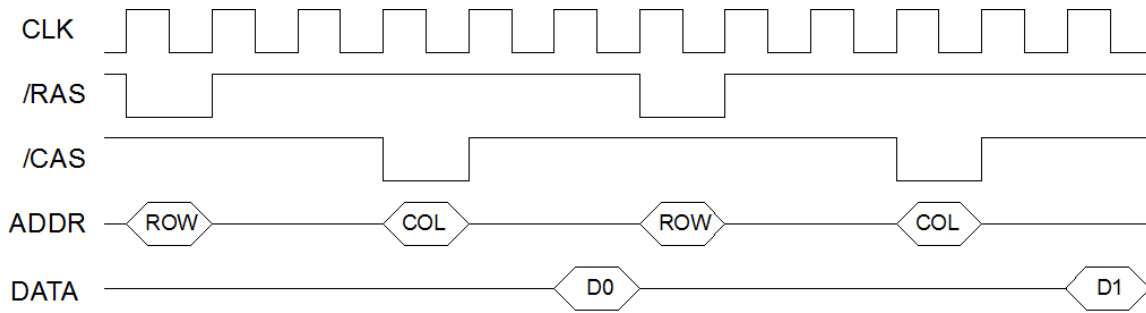

2M x 8 bit memory (internal view)

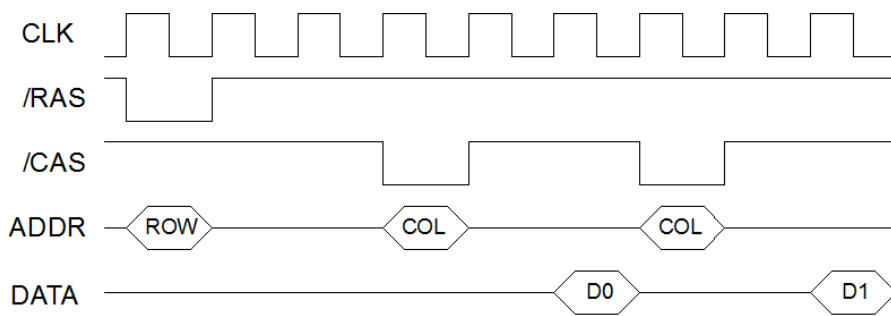* note that D0 – D7 are *bits* of data

Async DRAM read (2 words)

CLK

/RAS

/CAS

ADDR ROW   COL   ROW   COL

DATA   D0   D1

Async DRAM FPM read (2 words)

CLK

/RAS

/CAS

ADDR ROW   COL   COL

DATA   D0   D1

SDRAM read (2 word burst)

CLK

/RAS

/CAS

ADDR ROW   COL

DATA   D0 D1
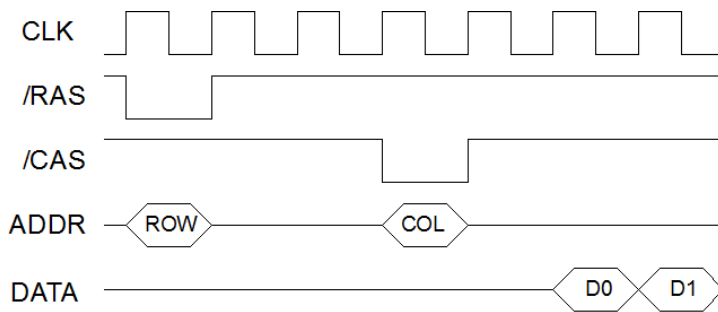
SDRAM DDR read (2 word burst)

CLK

/RAS

/CAS

ADDR ROW   COL

DATA   D0 D1
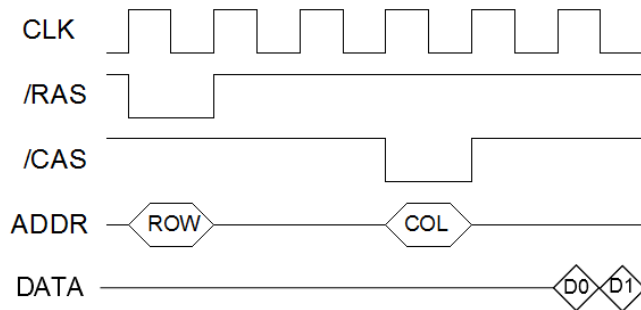
** note that D0 and D1 are *words* of data