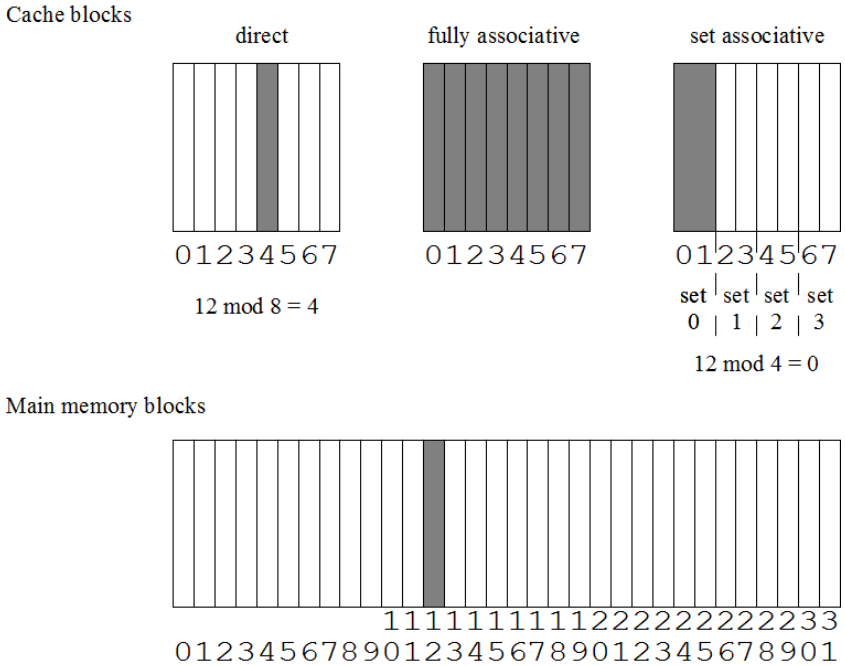
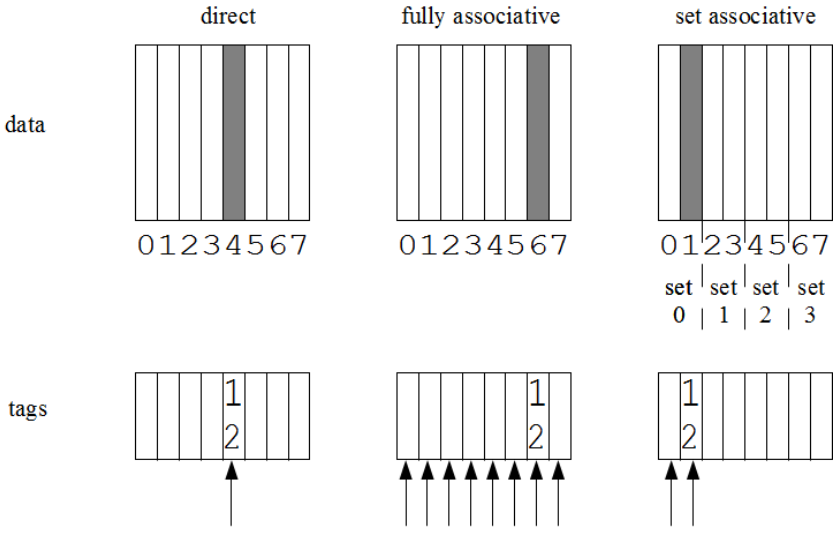
Cache Mapping Technique*



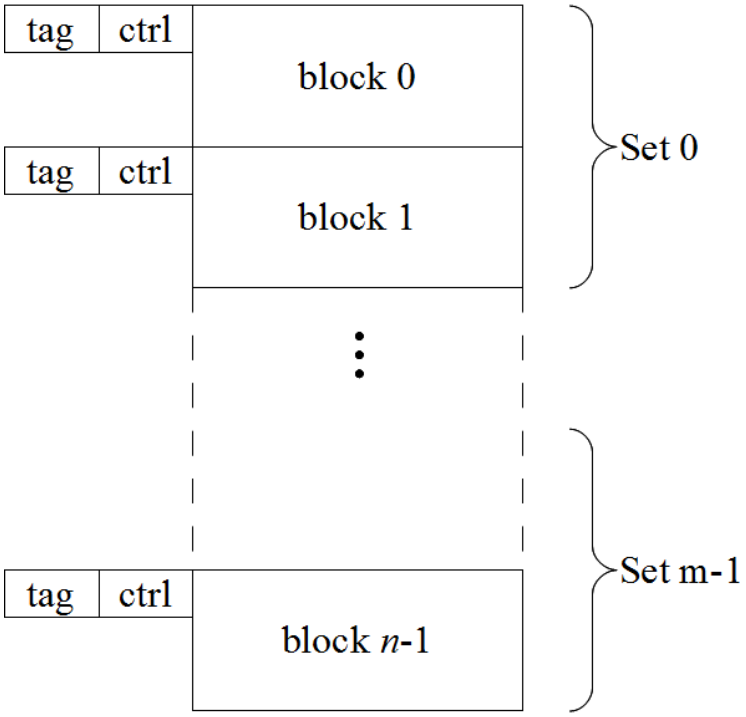
*adapted from figures in Hennessy and Patterson's Computer Architecture

Cache Searching*



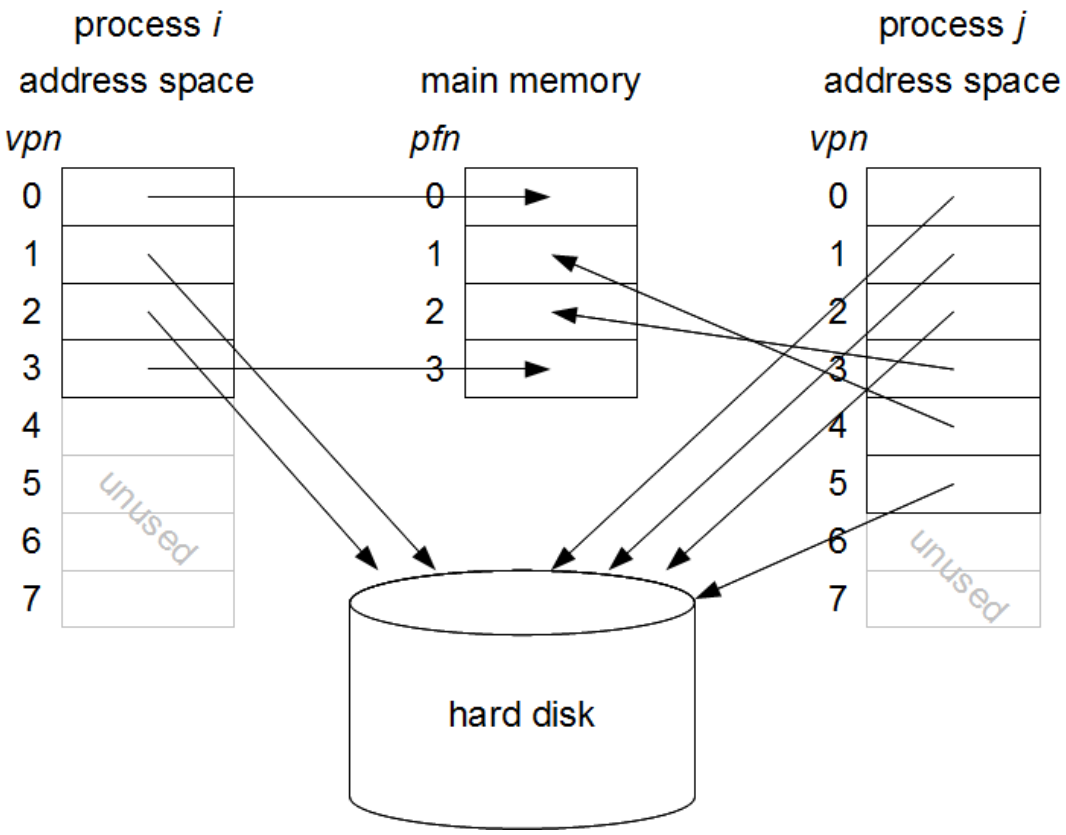
*adapted from figures in Hennessy and Patterson's Computer Architecture

Cache Organization



tag: identifies source block in main memory
ctrl: control bits (*v* – valid, *d* – dirty, ...)

Virtual Memory for 2 Processes



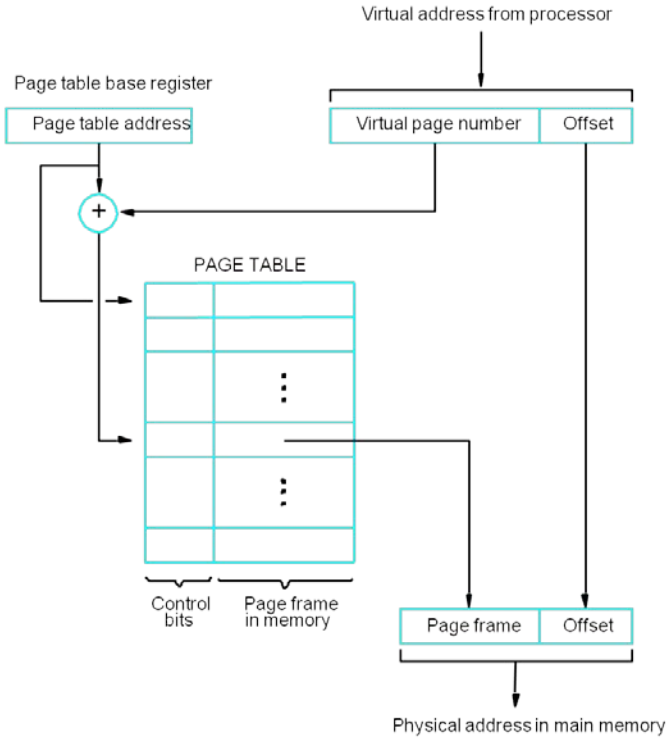


Figure 5.27. Virtual-memory address translation.
8.25

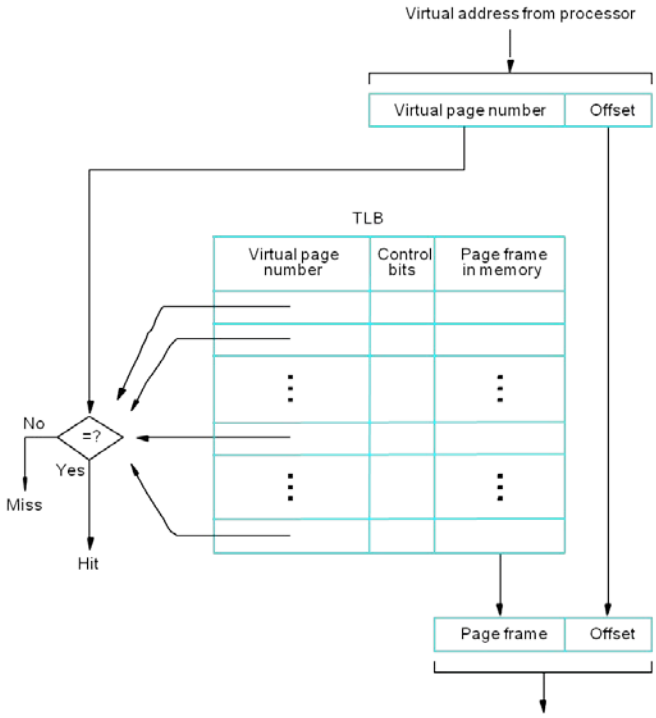


Figure 5.28. Use of an associative-mapped TLB.
8.26